CLAIMS

What is claimed is:

1. A method for forming a damascene structure to improve a chemical mechanical polishing (CMP) process while reducing the capacitance in an integrated circuit comprising the steps of:

providing a semiconductor substrate comprising a dielectric insulating layer including a first damascene opening;

blanket depositing a first resist layer to fill the first damascene opening and patterning the first resist layer to form an etching mask for etching a dummy damascene opening adjacent the first damascene opening;

etching the dummy damascene opening into a thickness portion of the dielectric insulating layer;

blanket depositing a bottom anti-reflective coating (BARC) layer to include filling the dummy damascene opening;

forming a second damascene opening through a thickness portion of the dielectric insulating layer to at least partially encompass the first damascene opening;

removing the BARC layer to exposed the dummy damascene opening;

forming a metal layer to include filling the first and second damascene openings and the dummy damascene opening; and,

planarizing the metal layer according to a CMP process to include removing a portion of the dielectric insulating layer greater than the dummy damascene opening depth to remove the dummy damascene.

2. The method of claim 1, wherein the step of forming a second damascene opening comprises depositing and patterning a second resist layer to form an etching mask for etching the second damascene opening.

3. The method of claim 2, wherein the second resist layer comprises a deep ultraviolet (DUV) photoresist.

4. The method of claim 1, wherein the first and second damascene openings are selected from the group consisting of a via opening and a trench opening.

5. The method of claim 1, wherein the second damascene opening comprises a trench portion of a dual damascene structure.

6. The method of claim 1, wherein the second damascene opening is formed to a depth greater than the dummy damascene opening.

7. The method of claim 1, wherein the first damascene opening is a via opening.

8. The method of claim 1, wherein the BARC layer is selected from the group consisting of a resinous polymer, a spin-on glass, a spin-on dielectric, and a CVD dielectric.

9. The method of claim 1, wherein the semiconductor substrate further comprises a dielectric anti-reflectance coating (DARC) layer overlying the dielectric insulating layer.

10. The method of claim 1, wherein the first damascene opening comprises one of a diameter or width less than about 0.25 microns.

11. The method of claim 1, wherein the metal layer is selected from the group consisting of tungsten aluminum, copper and alloys thereof.

12. The method of claim 1, wherein the metal layer comprises copper and alloys thereof.

13. The method of claim 1, wherein the dielectric insulating layer comprises a low-K silicon oxide based material.

14. The method of claim 1, wherein the dielectric insulating layer is selected from the group consisting of organo-silicate glass, and carbon doped silicon oxide.

15. A method for forming a dummy damascene structure to improve a chemical mechanical polishing (CMP) process while reducing the capacitance in a multi-level integrated circuit comprising the steps of:

forming a first via opening through a thickness portion of a dielectric insulating layer having an overlying dielectric anti-reflectance coating (DARC) layer;

blanket depositing a first resist layer to fill the damascene opening and patterning the first resist layer to form an etching mask for etching a dummy damascene opening adjacent the via opening;

etching the dummy damascene opening through a thickness portion of the dielectric insulating layer to a first depth;

blanket depositing a bottom anti-reflective coating (BARC) layer to include filling the dummy damascene opening;

forming a damascene opening to a second depth greater than the first depth through a thickness portion of the dielectric insulating layer to at least partially encompass the via opening;

removing the BARC layer to exposed the dummy damascene opening;

forming a metal layer to include filling the via opening, damascene opening, and the dummy damascene opening; and,

planarizing the metal layer according to a CMP process to include removing a portion of the dielectric insulating layer greater than the dummy damascene opening depth to remove the dummy damascene.

16. The method of claim 15, wherein the step of forming a damascene opening comprises depositing and patterning a second resist layer to form an etching mask for etching the damascene opening.

17. The method of claim 16, wherein the second resist layer comprises a deep ultraviolet (DUV) photoresist.

18. The method of claim 15, wherein the damascene opening is selected from the group consisting of a via opening and a trench opening.

19. The method of claim 15, wherein the damascene opening comprises a trench portion of a dual damascene structure.

20. The method of claim 15, wherein the BARC layer is selected from the group consisting of a resinous polymer, a spin-on glass, a spin-on dielectric, and a CVD dielectric.

21. The method of claim 15, wherein the via opening comprises a diameter of less than about 0.25 microns.

22. The method of claim 15, wherein the metal layer is selected from the group consisting of tungsten aluminum, copper and alloys thereof.

23. The method of claim 15, wherein the metal layer comprises copper and alloys thereof.

24. The method of claim 15, wherein the dielectric insulating layer comprises a low-K silicon oxide based material.

25. The method of claim 15, wherein the dielectric insulating layer is selected from the group consisting of organo-silicate glass, and carbon doped silicon oxide.

26. A method for forming a dummy damascene structure to improve a chemical mechanical polishing (CMP) process while reducing the capacitance in a multi-level integrated circuit comprising the steps of:

forming a first damascene opening through a thickness portion of a dielectric insulating layer;

forming a dummy damascene opening adjacent the first damascene opening through a thickness portion of the dielectric insulating layer to a first depth;

forming a second damascene opening to a second depth greater than the first depth through a thickness portion of the dielectric insulating layer to at least partially encompass the via opening;

forming a metal layer to include filling the first and second damascene openings and the dummy damascene opening; and,

planarizing the metal layer according to a CMP process to include removing a portion of the dielectric insulating layer greater than the dummy damascene opening depth to remove the dummy damascene while leaving a portion of the second damascene opening.